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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/923,341	08/08/2001	Gillian F. Marshall	124-880	2769

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EXAMINER	
NGUYEN, JOSEPH H	
ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 07/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/923,341	MARSHALL ET AL.	
	Examiner	Art Unit	
	Joseph Nguyen	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7-12,38,39 and 41-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-12,38,39 and 41-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 7, 51, 52, 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over figure 13B of Sahara et al in view of figure 8B of Sahara et al.

Regarding claims 1, 51 and 52, 53, Sahara et al discloses on figure 13B substantially all the structures steps of the method set forth in the claimed invention except a deposited epitaxial layer supported by said CMOS component. However, Sahara et al discloses on figure 8B a deposited epitaxial layer 13 supported by said CMOS component. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify figure 13B of Sahara et al by having a deposited epitaxial layer supported by said CMOS component for the purpose of providing higher speed application in a photodetector circuit.

Note that Sahara et al discloses on figure 13B a layer 164 is supported by said CMOS component, said layer providing only one of said active regions, said photodiode detector. However, this layer is not a deposited epitaxial layer. Further, the limitation of "in response to said only one active region, having a gradual knee in a current voltage

characteristic" is merely the functional language and thus is not given a patentable weight.

Regarding claim 7, Sahara et al discloses on figure 13B the photo-circuit is arranged to provide a logarithmic response to incident radiation.

Claims 2, 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over figure 13B of Sahara et al and figure 8B of Sahara et al as applied to claim 1 above, and further in view of Inoue et al.

Regarding claim 2, Sahara et al discloses on figures 13B and 8B substantially all the structure set forth in the claimed invention except a substrate insulated from CMOS circuit. However, Inoue et al discloses on figure 2 a substrate 101 insulated from CMOS circuit 117. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify figure 13B of Sahara et al and figure 8B of Sahara et al by having a substrate insulated from CMOS circuit for the purpose of reducing the leakage current in a CMOS photodiode device.

Regarding claim 4, figure 13B of Sahara et al and figure 8B of Sahara et al and Inoue et al together disclose the structure set forth in claim 4.

Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over figure 13B of Sahara et al and figure 8B of Sâhara et al as applied to claim 1 above, and further in view of Okabayashi et al.

Regarding claim 8, Sahara et al discloses on figures 13B and 8B substantially all the structure set forth in the claimed invention except parasitic photo-diodes arranged in series with said readout circuit for contributing to circuit output in response to incident radiation. However, Okabayashi et al discloses on figure 10 parasitic photo-diodes arranged in series with said readout circuit for contributing to circuit output in response to incident radiation. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sahara et al by having parasitic photo-diodes arranged in series with said readout circuit for contributing to circuit output in response to incident radiation for the purpose of increasing the signal to noise ratio as taught by Okabayashi et al (col. 2, lines 47-48).

Regarding claim 9, Sahara et al disclose substantially all the structure set forth in the claimed invention except amplifier arranged in a feedback loop for providing feedback to stabilize photo-diode detector bias voltage. However, Okabayashi et al discloses on figure 10 amplifier arranged in a feedback loop for providing feedback to stabilize photo-diode detector bias voltage. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sahara et al by having amplifier arranged in a feedback loop for providing feedback to stabilize photo-diode detector bias voltage for the purpose of increasing the signal to noise ratio as taught by Okabayashi et al (col. 2, lines 47-48).

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over figure 13B of Sahara et al and figure 8B of Sahara et al and Okabayashi et al as applied to claim 9 above, and further in view of Fossum et al.

Regarding claim 10, figure 13B of Sahara et al and figure 8B of Sahara et al and Okabayashi et al disclose substantially all the structure set forth in the claimed invention except a load transistor. However, Fossum et al discloses a load transistor. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify figure 13B of Sahara et al and figure 8B of Sahara et al and Okabayashi et al by having a load transistor for the purpose of improving the performance of a CMOS photo-diode device.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over figure 13B of Sahara et al and figure 8B of Sahara et al and Okabayashi et al and Fossum et al as applied to claim 10 above, and further in view of Uchida et al.

Regarding claim 11, figure 13B of Sahara et al and figure 8B of Sahara et al and Okabayashi et al and Fossum et al disclose substantially all the structure set forth in the claimed invention except the amplifier being a push pull amplifier. However, Uchida et al discloses a push pull amplifier (col. 2, line 41). In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify figure 13B of Sahara et al and figure 8B of Sahara et al and Okabayashi et al and Fossum et al by having the amplifier being a push pull amplifier for the purpose of improving the performance of a CMOS photo-diode device.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over figure 13B of Sahara et al and figure 8B of Sahara et al and Okabayashi et al and Fossum et al as applied to claim 10 above, and further in view of Kozlowski.

Regarding claim 12, figure 13B of Sahara et al and figure 8B of Sahara et al and Okabayashi et al and Fossum et al disclose substantially all the structure set forth in the claimed invention except a cascode transistor. However, Kozlowski discloses on figure 3 a cascode transistor Q28. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sahara et al and Okabayashi et al and Fossum et al by having would have been obvious to one of ordinary skill in the art at the time the invention was made to modify figure 13B of Sahara et al and figure 8B of Sahara et al and Okabayashi et al and Fossum et al by having a cascode transistor for the purpose of improving the performance of a CMOS photo-diode device.

Claim 38, 41-43, 54 is rejected under 35 U.S.C. 103(a) as being unpatentable over figure 13B of Sahara et al and figure 8B of Sahara et al in view of Cunningham et al.

Regarding claims 38, 41-43, 54, figure 13B of Sahara et al and figure 8B of Sahara et al disclose substantially all the structure or steps of the method set forth in the claimed invention except the photo-diode being a PIN structure. However, Cunningham et al discloses on figure 2 the photo-diode detector being a PIN structure

26. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify figure 13B of Sahara et al and figure 8B of Sahara et al by having the photo-diode being a PIN structure for the purpose of improving the performance of a CMOS photo-diode device.

Claims 39, 3, 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over figure 13B of Sahara et al and figure 8B of Sahara et al and Cunningham et al as applied to claim 38 above and further in view of Inoue et al.

Regarding claim 39, 3, 49, figure 13B of Sahara et al and figure 8B of Sahara et al and Cunningham et al disclose substantially all the structure set forth in the claimed invention except a substrate insulated from CMOS circuitry. However, Inoue et al discloses on figure 2 a substrate 101 insulated from CMOS circuitry 117. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify figure 13B of Sahara et al and figure 8B of Sahara et al and Cunningham et al by having a substrate insulated from CMOS circuitry for the purpose of reducing the leakage current in a CMOS photodiode device.

Claims 44-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over figure 13B of Sahara et al and figure 8B of Sahara et al and Cunningham et al as applied to claim 38 above and further in view of Okabayashi et al.

Regarding claim 44, Sahara et al and Cunningham et al disclose substantially all the structure set forth in the claimed invention except parasitic photo-diodes arranged to

contribute to circuit output in response to incident radiation. However, Okabayashi et al discloses on figure 10 parasitic photo-diodes arranged to contribute to circuit output in response to incident radiation. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify figure 13B of Sahara et al and figure 8B of Sahara et al and Cunningham et al by having parasitic photo-diodes arranged to contribute to circuit output in response to incident radiation for the purpose of increasing the signal to noise ratio as taught by Okabayashi et al (col. 2, lines 47-48).

Regarding claims 45-46, figure 13B of Sahara et al and figure 8B of Sahara et al and Cunningham et al disclose substantially all the structure set forth in the claimed invention except amplifier arranged to provide feedback to stabilize photo-diode detector. However, Okabayashi et al discloses on figure 10 amplifier arranged to provide feedback to stabilize photo-diode detector. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify figure 13B of Sahara et al and figure 8B of Sahara et al and Cunningham et al by having amplifier arranged to provided feedback to stabilize photo-diode detector for the purpose of increasing the signal to noise ratio as taught by Okabayashi et al (col. 2, lines 47-48).

Claim 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over figure 13B of Sahara et al and figure 8B of Sahara et al and Cunningham et al and Okabayashi et al as applied to claim 46 above and further in view of Uchiba et al.

Regarding claim 47, figure 13B of Sahara et al and figure 8B of Sahara et al and Cunningham et al and Okabayashi et al disclose substantially all the structure set forth in the claimed invention except the amplifier being a push pull amplifier. However, Uchida et al discloses a push pull amplifier (col. 2, line 41). In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify figure 13B of Sahara et al and figure 8B of Sahara et al and Cunningham et al and Okabayashi et al by having the amplifier being a push pull amplifier for the purpose of improving the performance of a CMOS photo-diode device.

Claim 48 is rejected under 35 U.S.C. 103(a) as being unpatentable over figure 13B of Sahara et al and figure 8B of Sahara et al and Cunningham et al and Okabayashi et al as applied to claim 46 above and further in view of Kozlowski.

Regarding claim 48, figure 13B of Sahara et al and figure 8B of Sahara et al and Cunningham et al and Okabayashi et al disclose substantially all the structure set forth in the claimed invention except a cascode transistor. However, Kozlowski discloses on figure 3 a cascode transistor Q28. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify figure 13B of Sahara et al and figure 8B of Sahara et al and Cunningham et al and Okabayashi et al by having would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sahara et al and Cunningham et al Okabayashi et al by having a cascode transistor for the purpose of improving the performance of a CMOS photo-diode device.

Claim 50 is rejected under 35 U.S.C. 103(a) as being unpatentable over figure 13B of Sahara et al and figure 8B of Sahara et al and Cunningham et al as applied to claim 49 above and further in view of Morikawa et al.

Regarding claim 50, figure 13B of Sahara et al and figure 8B of Sahara et al and Cunningham et al disclose substantially all the structure set forth in the claimed invention except the undoped epitaxial layer being of SiGe alloy. However, Morikawa et al discloses on figure 3A the undoped epitaxial layer 14 being of SiGe. In view of such teaching, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify figure 13B of Sahara et al and figure 8B of Sahara et al and Cunningham et al by having the undoped epitaxial layer being of SiGe alloy for the purpose of improving the performance of a CMOS photo-diode device.

Response to Arguments

Applicant's arguments with respect to claims 1-4,7-12,38-39,41-54 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (703) 308-1269. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 308-7382 for regular communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JN
July 8, 2003

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